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Park

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(54) **APPARATUS FOR SIMPLIFICATION OF INPUT SIGNAL**

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H03K 5/1534   (2006.01)
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CPC *H03K 21/026* (2013.01); *H03K 5/1534* (2013.01)

(58) **Field of Classification Search**
CPC H03K 21/02
See application file for complete search history.

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(57)   **ABSTRACT**

The present disclosure relates to an apparatus for simplification of input signal configured to simplify a process of microprocessor and to enhance a speed by transforming six input modes of 1-phase/2-input/1-multiplication mode, 1-phase/2-input/2-multiplication mode, CW/CCW mode, 2-phase/1-multiplication mode, 2-phase/2-multiplication mode and 2-phase/4-multiplication mode to a same shape according to types of encoder connected to a PLC high speed counter, and transmitting to the microprocessor, and by adding the six types of input modes to a logic gate circuit of a high speed counter input circuit.
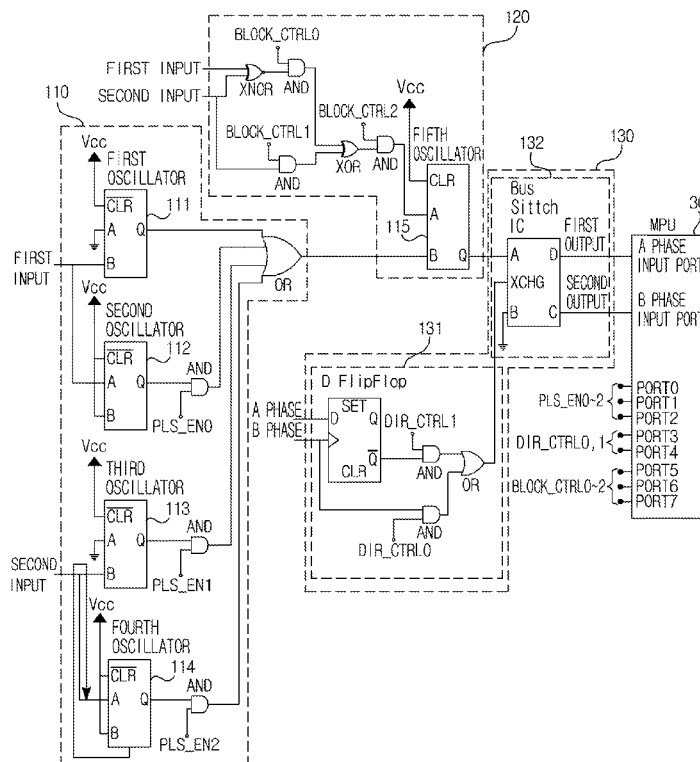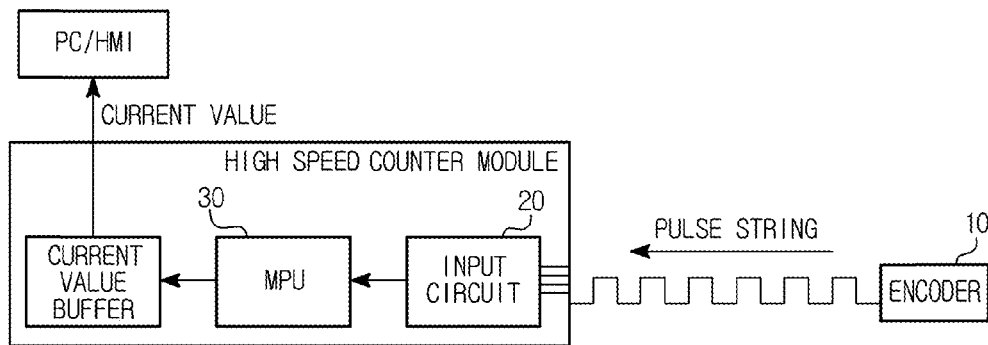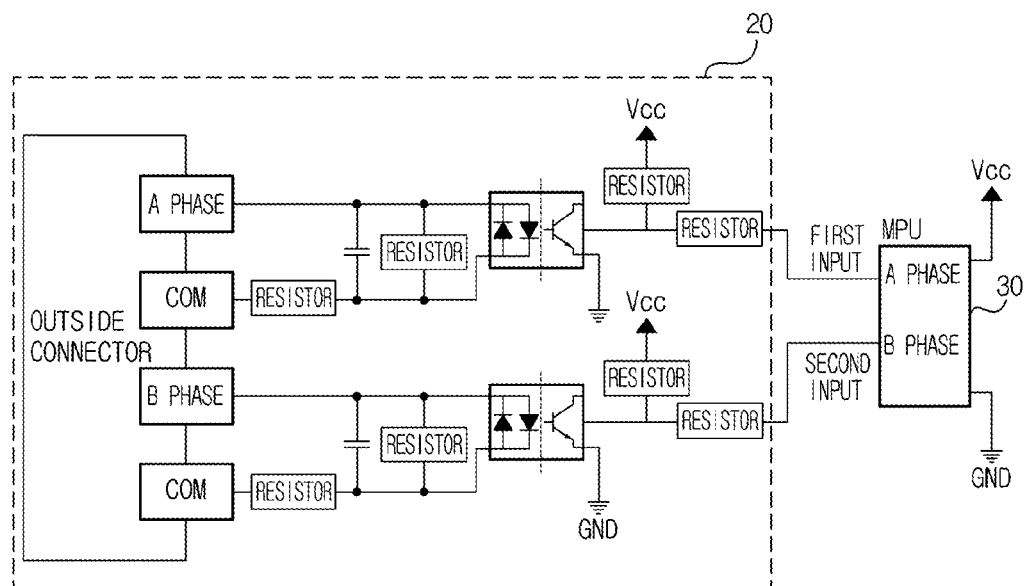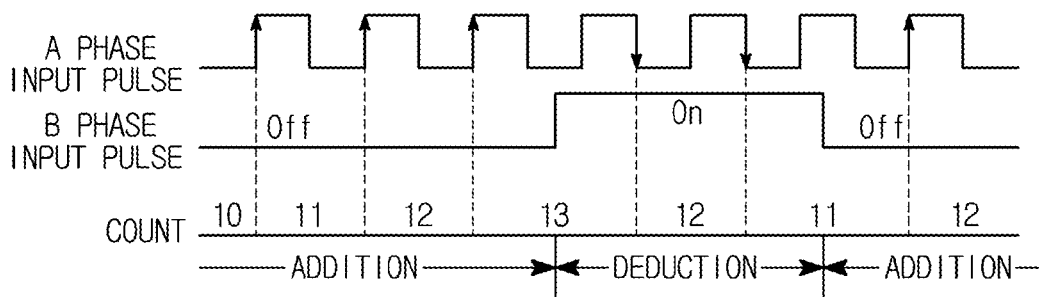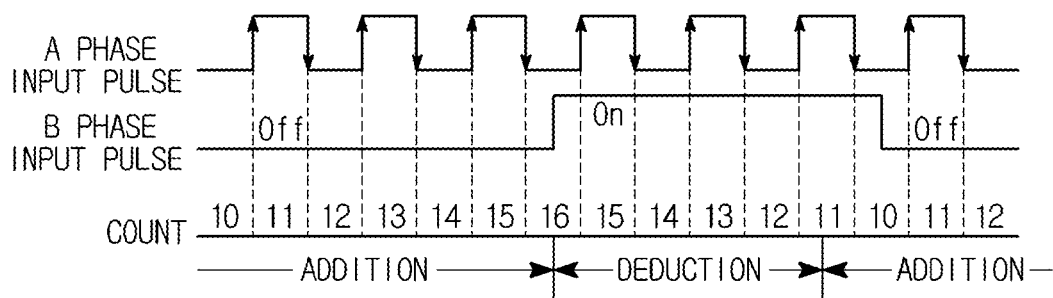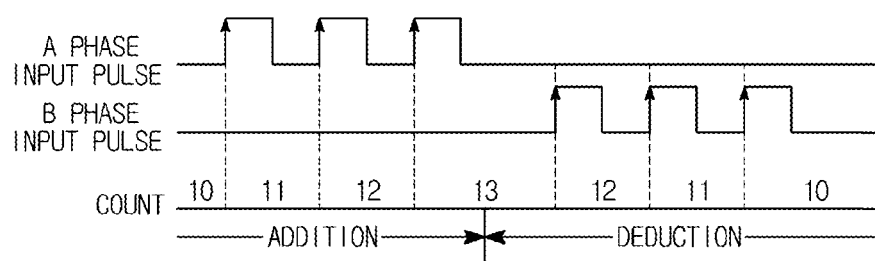
7 Claims, 16 Drawing Sheets

FIG. 1
(PRIOR ART)

FIG. 2
(PRIOR ART)

FIG. 3a
(PRIOR ART)

ADDITION/DEDUCTION COUNT CLASSIFICATION	A PHASE PULSE RISE	A PHASE PULSE FALL
B PHASE INPUT PULSE Off	ADDITION COUNT(+1)	–
B PHASE INPUT PULSE On	–	DEDUCTION COUNT(−1)

FIG. 3b
(PRIOR ART)

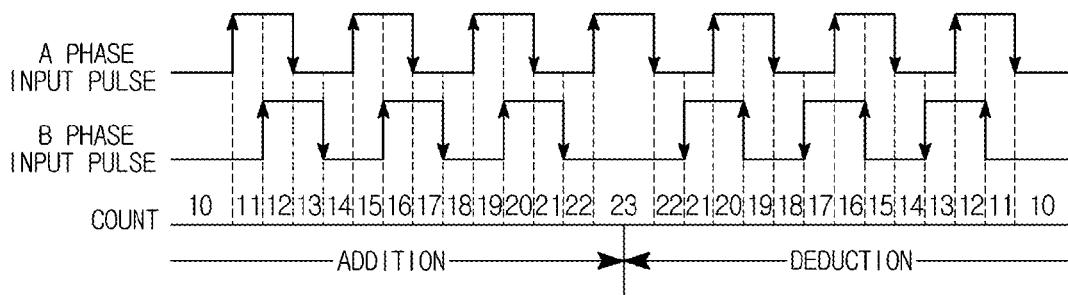| ADDITION/DEDUCTION COUNT CLASSIFICATION	A PHASE PULSE RISE	A PHASE PULSE FALL
B PHASE INPUT PULSE Off	ADDITION COUNT(+1)	ADDITION COUNT(+1)
B PHASE INPUT PULSE On	DEDUCTION COUNT(−1)	DEDUCTION COUNT(−1)

FIG. 3c
(PRIOR ART)

ADDITION/DEDUCTION COUNT CLASSIFICATION	A PHASE PULSE RISE	A PHASE PULSE FALL	B PHASE PULSE RISE	B PHASE PULSE FALL
B PHASE INPUT PULSE Off	ADDITION COUNT(+1)	—	—	—
A PHASE INPUT PULSE Off	—	—	DEDUCTION COUNT(−1)	—

FIG. 3d
(PRIOR ART)
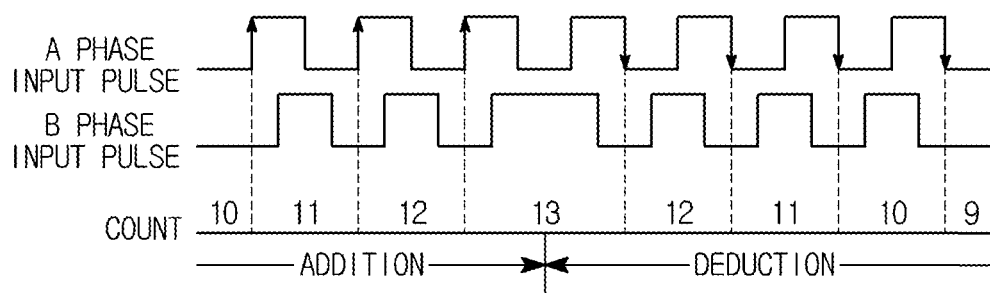
ADDITION/DEDUCTION COUNT CLASSIFICATION	A PHASE PULSE RISE	A PHASE PULSE FALL
PHASE OF A PHASE AND PHASE OF B PHASE (A PHASE ~ B PHASE)	ADDITION COUNT(+1)	—
PHASE OF A PHASE AND PHASE OF B PHASE (B PHASE ~ A PHASE)	—	DEDUCTION COUNT(-1)

FIG. 3e
(PRIOR ART)
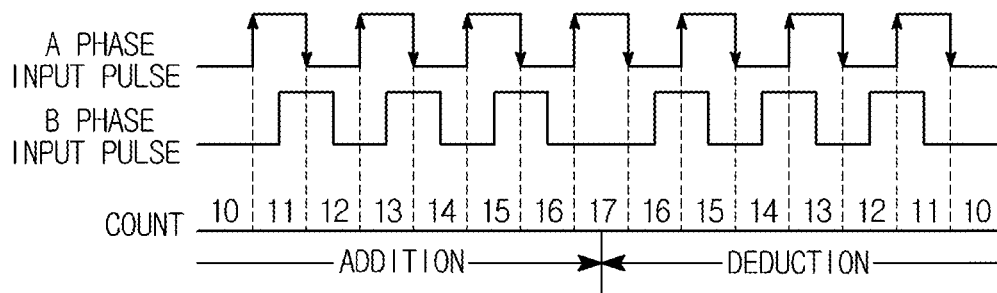
A PHASE
INPUT PULSE

B PHASE
INPUT PULSE

COUNT　10 ¦ 11 ¦ 12 ¦ 13 ¦ 14 ¦ 15 ¦ 16 ¦ 17 ¦ 16 ¦ 15 ¦ 14 ¦ 13 ¦ 12 ¦ 11 ¦ 10

———————ADDITION———————▶◀———————DEDUCTION———————

ADDITION/DEDUCTION COUNT CLASSIFICATION	A PHASE PULSE RISE	A PHASE PULSE FALL
PHASE OF A PHASE AND PHASE OF B PHASE (A PHASE - B PHASE)	ADDITION COUNT(+1)	ADDITION COUNT(+1)
PHASE OF A PHASE AND PHASE OF B PHASE (B PHASE - A PHASE)	DEDUCTION COUNT(-1)	DEDUCTION COUNT(-1)

FIG. 3f
(PRIOR ART)

| ADDITION/DEDUCTION COUNT CLASSIFICATION	A PHASE PULSE RISE	A PHASE PULSE FALL	B PHASE PULSE RISE	B PHASE PULSE FALL
PHASE OF A PHASE AND PHASE OF B PHASE (A PHASE - B PHASE)	ADDITION COUNT(+1)	ADDITION COUNT(+1)	ADDITION COUNT(+1)	ADDITION COUNT(+1)
PHASE OF A PHASE AND PHASE OF B PHASE (B PHASE - A PHASE)	DEDUCTION COUNT(-1)	DEDUCTION COUNT(-1)	DEDUCTION COUNT(-1)	DEDUCTION COUNT(-1)

FIG. 4a
(PRIOR ART)
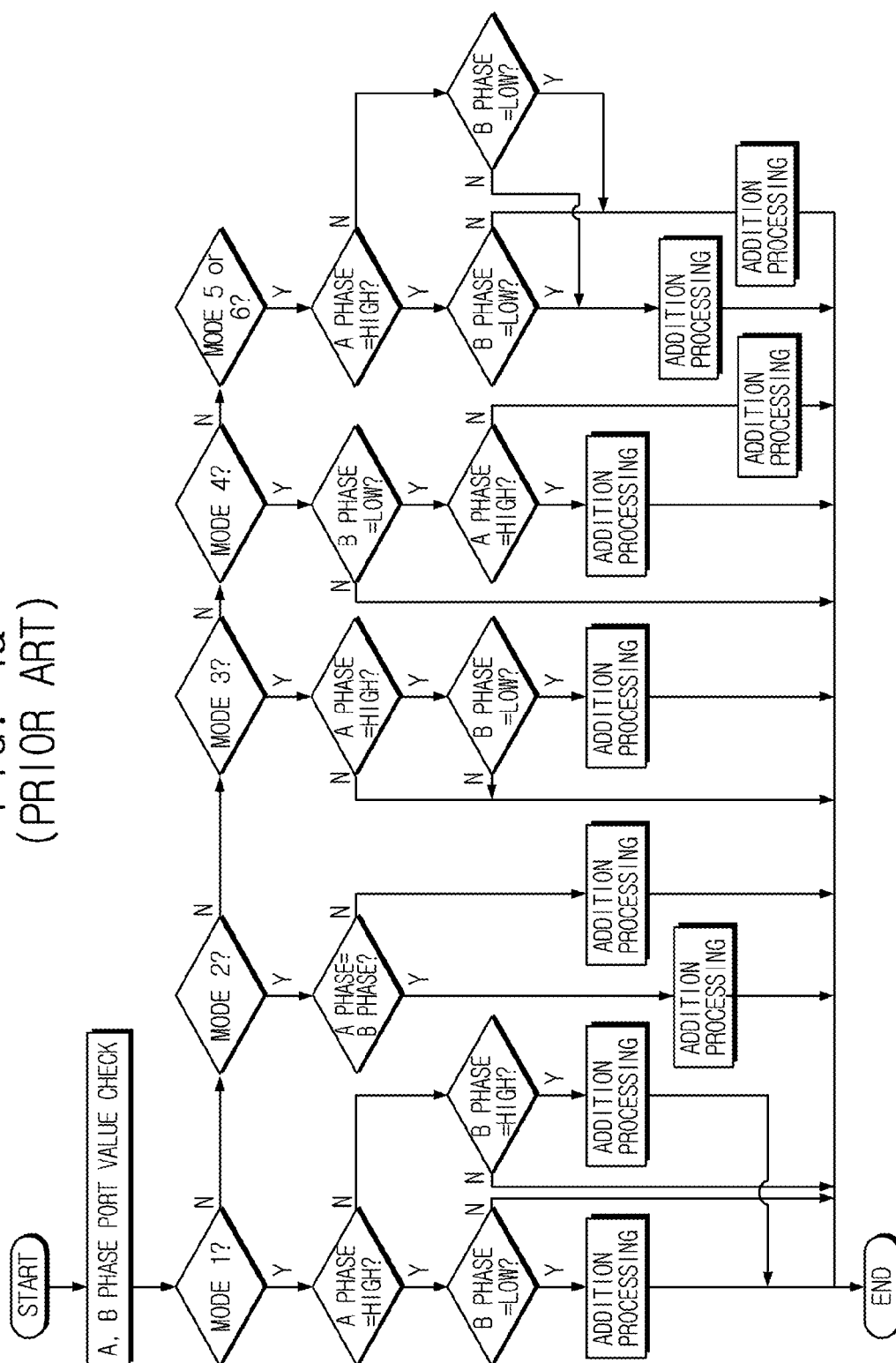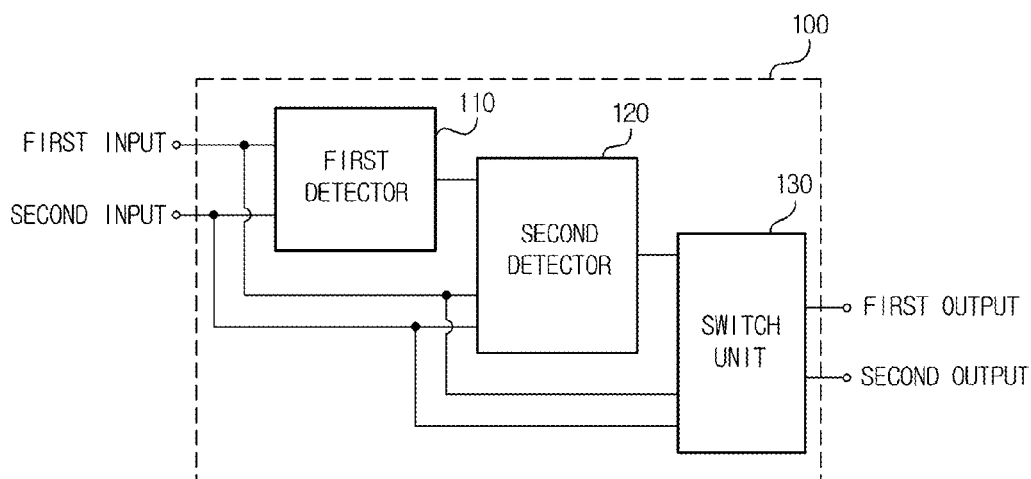
FIG. 4b
(PRIOR ART)
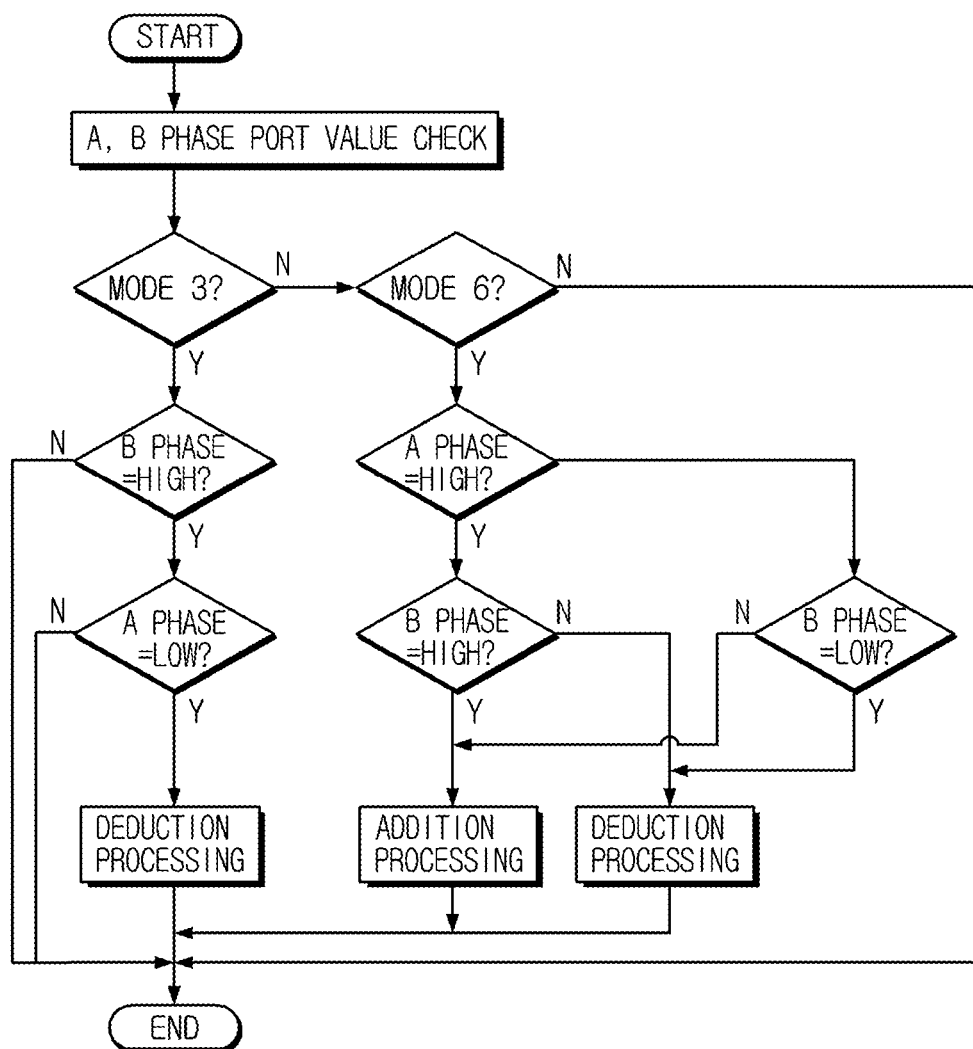
FIG. 5
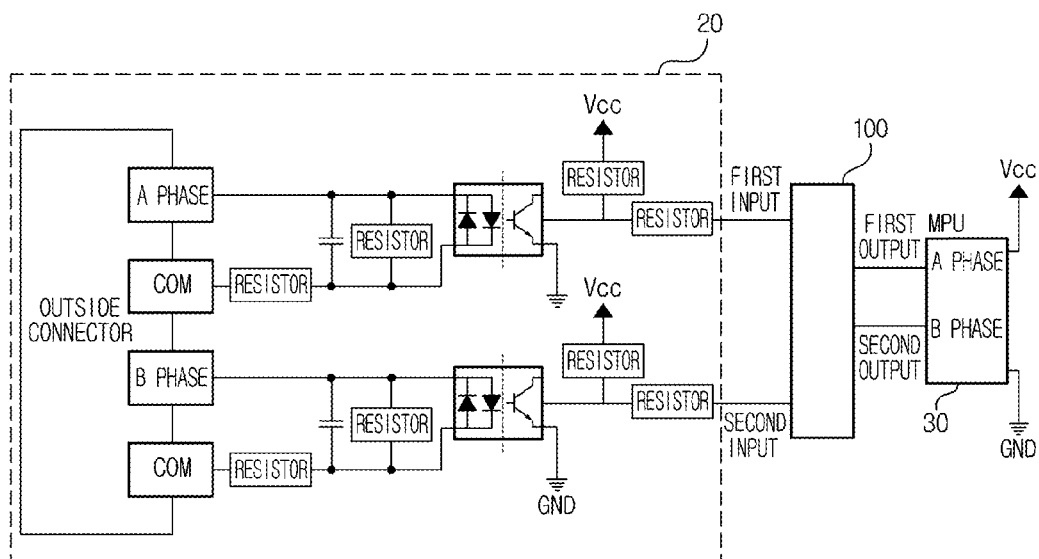
FIG. 6

FIG. 7a
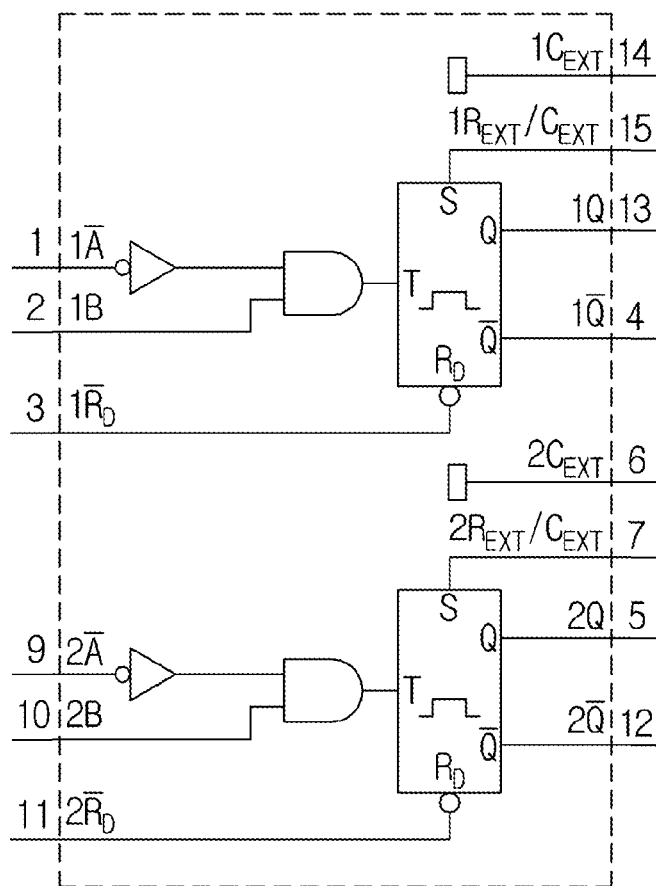
FIG. 7b

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	$L^{(2)}$	$H^{(2)}$
X	X	L	$L^{(2)}$	$H^{(2)}$
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔

FIG. 8a
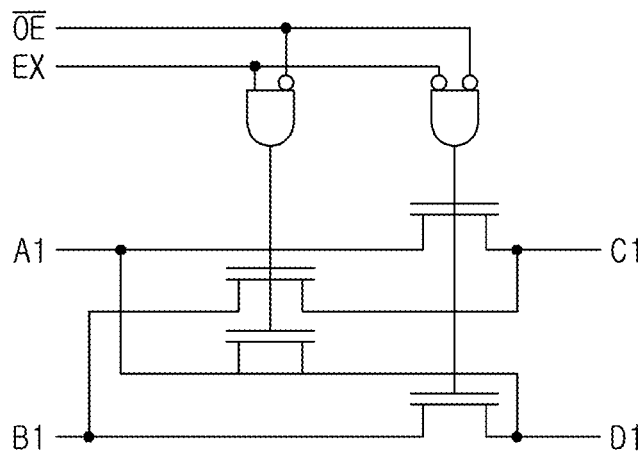
FIG. 8b

$\overline{OE}$	EX	A1	B1	C1	D1	Funotion
H	X	HI-Z				Disconnect
L	L	A1 – C1, B1 – D1				Connect
L	H	A1 – D1, B1 – C1				Exchange

FIG. 9
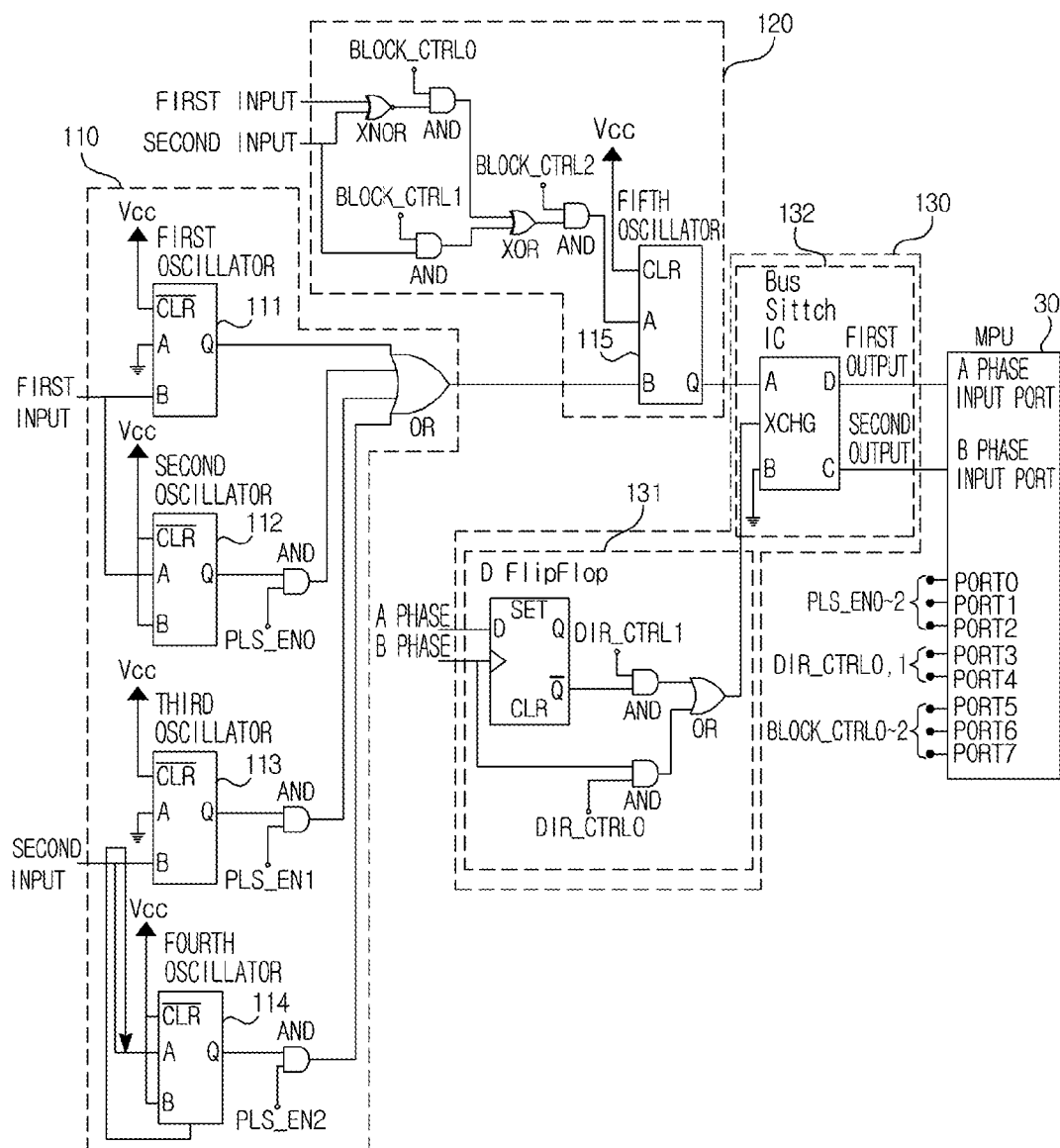
FIG. 10

MODE	PLS_EN0	PLS_EN1	PLS_EN2	DIR_CTRL0	DIR_CTRL1	BLOCK_CTRL0	BLOCK_CTRL1	BLOCK_CTRL2
FIRST MODE	1	0	0	1	0	1	0	1
SECOND MODE	1	0	0	1	0	X (ARBITRARY VALUE)	X (ARBITRARY VALUE)	0
THIRD MODE	0	1	0	1	0	1	0	1
FOURTH MODE	1	0	0	0	1	0	1	1
FIFTH MODE	1	0	0	0	1	X (ARBITRARY VALUE)	X (ARBITRARY VALUE)	0
SIXTH MODE	1	1	1	0	1	X (ARBITRARY VALUE)	X (ARBITRARY VALUE)	0

FIG. 11

1 PHASE/2 INPUT/1 MULTIPLIFICATION
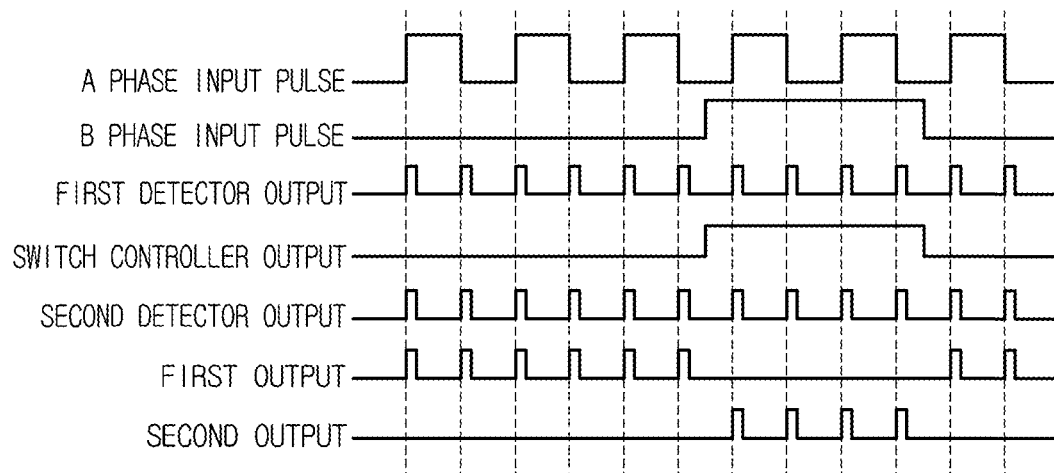
FIG. 12

1 PHASE/2 INPUT/2 MULTIPLICATION

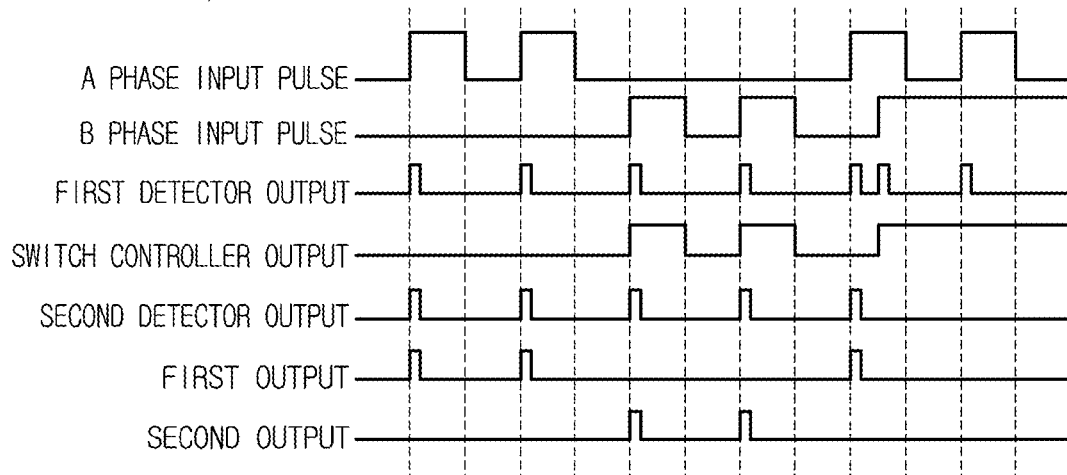A PHASE INPUT PULSE

B PHASE INPUT PULSE

FIRST DETECTOR OUTPUT

SWITCH CONTROLLER OUTPUT

SECOND DETECTOR OUTPUT

FIRST OUTPUT

SECOND OUTPUT

FIG. 13

CW/CCW MODE

A PHASE INPUT PULSE

B PHASE INPUT PULSE

FIRST DETECTOR OUTPUT

SWITCH CONTROLLER OUTPUT

SECOND DETECTOR OUTPUT

FIRST OUTPUT

SECOND OUTPUT

FIG. 14

2 PHASE/1 MULTIPLICATION

A PHASE INPUT PULSE

B PHASE INPUT PULSE

FIRST DETECTOR OUTPUT

SWITCH CONTROLLER OUTPUT

SECOND DETECTOR OUTPUT

FIRST OUTPUT

SECOND OUTPUT

FIG. 15

2 PHASE/2 MULTIPLICATION

A PHASE INPUT PULSE

B PHASE INPUT PULSE

FIRST DETECTOR OUTPUT

SWITCH CONTROLLER OUTPUT

SECOND DETECTOR OUTPUT
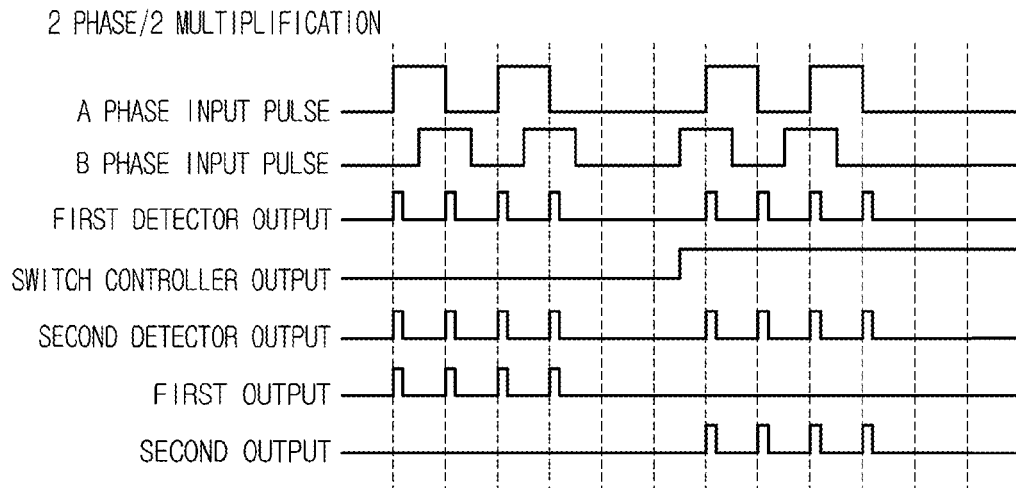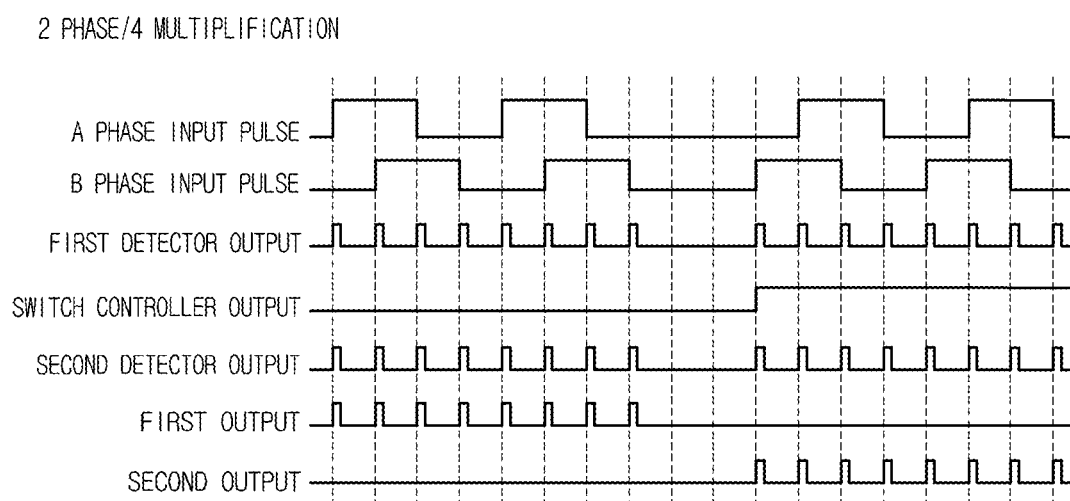
FIRST OUTPUT

SECOND OUTPUT

FIG. 16

2 PHASE/4 MULTIPLICATION

APPARATUS FOR SIMPLIFICATION OF INPUT SIGNAL

Pursuant to 35 U.S.C. §119 (a), this application claims the benefit of earlier filing date and right of priority to Korean Patent Application No. 10-2013-0159121, filed on Dec. 19, 2013, the contents of which are hereby incorporated by reference in their entirety.

BACKGROUND OF THE DISCLOSURE

1. Field of Endeavor

Exemplary embodiments of the present disclosure generally relate to an apparatus for simplification of input signal.

2. Background

The information disclosed in this Discussion of the Related Art section is only for enhancement of understanding of the general background of the present disclosure and should not be taken as an acknowledgement or any form of suggestion that this information forms the prior art already known to a person skilled in the art.

Generally, a high speed counter module of PLC (Programmable Logic Controller) is a module configured to function to count a fast pulse signal of a pulse generator or an encoder that cannot be counted by a general counter command.

FIG. 1 is a block diagram illustrating a configuration of a PLC high speed counter according to prior art.

Referring to FIG. 1, an input circuit (20) converts a high speed pulse signal generated by an encoder (10) to CMOS level signal for transmission to an outside interrupt port of an MPU (Micro Processor Unit, 30). The MPU (30) adds, deducts or disregards without any operation, a current value in response to a pulse input mode of the encoder (10) when a signal of the outside interrupt port connected to the input circuit (20) rises or falls, i.e., at a rising edge or a falling edge.

FIG. 2 is a block diagram illustrating an input circuit (20) of a PLC high speed counter according to prior art.

Referring to FIG. 2, signals of A-phase and B-phase of encoder (10) from outside connector is converted to a CMOS signal, which is in turn transmitted to A-phase and B-phase outside interrupt ports of MPU (30).

FIGS. 3a and 3f are schematic views illustrating six different input modes and operations thereof according to types of encoder (10). Hereinafter, a first mode refers to 1-phase/2-input/1-multiplication mode, a second mode refers to 1-phase/2-input/2-multiplication mode, a third mode refers to CW (Clockwise)/CCW (Counterclockwise) mode, a fourth mode refers to 2-phase/1-multiplication, a fifth mode refers to 2-phase/2-multiplication, and a sixth mode refers to 2-phase/4-multiplication, for convenience sake. The detailed operation of the first to sixth modes will be explained later.

FIG. 4 is a flow chart illustrating a flow of processing an interrupt according to prior art when the interrupt is generated in an outside interrupt ports of MPU (30) in the PLC high speed counter. FIG. 4a illustrates a case where an interrupt is generated on A phase, and FIG. 4b illustrates a case where an interrupt is generated on B phase.

Referring to FIGS. 4a and 4b, when an interrupt is generated on A phase, the MPU (30) operates in a method of determining by repeating at every time at which mode among first to sixth modes the interrupt is generated. Furthermore, when an interrupt is generated on B phase, the MPU (30) operates in a method of determining by repeating at every time at which mode between third mode and sixth

mode the interrupt is generated. Thus, when an interrupt is generated, the MPU (30) determines by repeating at every time to what mode an input mode corresponds.

Meantime, the MPU (30) temporarily stops the PLC scan program whenever a rising edge or a falling edge of an input signal connected to an outside interrupt port is detected, and performs a high speed counter processing routine after the interrupt is generated. Thus, when an edge of an input mode is detected according to the prior art, an interrupt processing time is lengthened in response to the performance of process shown in FIGS. 4a and 4b according to the input mode, and when a speed of input pulse string (train) increases, the resources of MPU is excessively and disadvantageously occupied due to delay in interrupt processing. Another disadvantage as a result thereof is that the processing speed of PLC scan program is slowed.

SUMMARY

The present disclosure has been made to solve the foregoing disadvantages/problems of the prior art and therefore an object of certain embodiments of the present invention is to provide an apparatus for simplification of input signal.

In one general aspect of the present disclosure, there is provided an apparatus for simplification of input signal configured to input, to an MPU (Micro Processing Unit), an output of an input circuit at a PLC high speed counter module by converting the input to a single signal, the apparatus comprising:

a first detector configured to output a single pulse in response to a rising edge or a falling edge by detecting the rising edge or the falling edge of a reference signal, which is a reference of adding or deducting calculation in response to an operation mode of the high speed counter module;

a second detector configured to detect, from an output of the first detector, a pulse of rising edge or falling edge configured to perform an actual adding or deducting calculation in response to an operation mode of the high speed counter module; and

a switching unit configured to output an output of the second detector using the adding or deducting calculation.

Preferably, but not necessarily, the first detector may include a first oscillation unit configured to output a signal pulse by detecting a rising edge of a first input, a second oscillation unit configured to output a signal pulse by detecting a falling edge of a first input, a third oscillation unit configured to output a signal pulse by detecting a rising edge of a second input, a fourth oscillation unit configured to output a signal pulse by detecting a falling edge of a second input, and an edge detector configured to detect only an output of a reference signal from the first to fourth oscillation units in response to the operation mode.

Preferably, but not necessarily, the operation mode may include any one mode of a first mode of 1-phase/2-input/1-multiplication method, a second mode of 1-phase/2-input/2-multiplication method, a third mode of CW/CCW method, a fourth mode of 2-phase/1-multiplication method, a fifth mode of 2-phase/2-multiplication method and a sixth mode of 2-phase/4-multiplication method.

Preferably, but not necessarily, the switching unit may include a 2-bit switch configured to perform a one-on-one connection or a cross connection in response to a control signal by receiving a 2-bit input, and a switch controller configured to control the 2-bit switch by outputting through adding or deducting calculation in response to the operation mode.

Preferably, but not necessarily, a control signal may be transmitted to the first, second detectors and the switching unit by using a general output port of the MPU.

Preferably, but not necessarily, the edge detector may remove an input which is not a reference signal in response to the operation mode.

Preferably, but not necessarily, the edge detector may combine outputs corresponding to the reference signal in response to the operation mode.

The apparatus for simplification of input signal according to the present disclosure has an advantageous effect in that interrupt processing of MPU can be simplified by simplification of high speed counter input signal. Another advantageous effect is that processing speed of adding or deducting calculation can be enhanced by simplification of interrupt process of the MPU.

Still another advantageous effect is that efficiency of MPU can be increased and interrupt process routine can be much simplified by selective transmission of only a pulse string to be transmitted per input mode in response to operation of mono-stable multi-vibrator and simple logic circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings show one or more exemplary embodiments in accordance with the present concepts, by way of example only, not by way of limitations. In the figures, like reference numerals refer to the same or similar elements.

Thus, a wide variety of potential practical and useful embodiments will be more readily understood through the following detailed description of certain exemplary embodiments, with reference to the accompanying exemplary drawings in which:

FIG. 1 is a configurative block diagram illustrating a PLC high speed counter according to prior art;

FIG. 2 is a general configurative block diagram illustrating an input circuit (20) in a PLC high speed counter according to prior art;

FIGS. 3a to 3f are schematic views illustrating six different input modes and operations thereof according to types of encoders;

FIGS. 4a and 4b are flow charts illustrating flows of processing a conventional interrupt when an interrupt is generated on an outside interrupt port of MPU (30) in a PLC high speed counter;

FIG. 5 is a configurative schematic view illustrating a PLC high speed counter included with an apparatus for simplification of input signal according to an exemplary embodiment of the present disclosure;

FIG. 6 is a configurative block diagram illustrating an apparatus (100) for simplification of input signal according to an exemplary embodiment of the present disclosure;

FIGS. 7a and 7b are schematic views illustrating each inner structure of first to fifth oscillation units (111, 112, 113, 114, 115) used in an apparatus (100) for simplification of input signal according to the present disclosure;

FIGS. 8a and 8b are schematic views illustrating an inner structure of 2-bit switch (132) of a switch unit (130) in an apparatus (100) for simplification of input signal and a truth table according to the present disclosure;

FIG. 9 is a schematic view illustrating an inner circuit of an apparatus (100) for simplification of input signal according to an exemplary embodiment of the present disclosure;

FIG. 10 is a schematic view illustrating a universal output port value, per input mode, of MPU (30) for logic circuit

control in an apparatus (100) for simplification of input signal according to an exemplary embodiment of the present disclosure;

FIGS. 11 to 16 are schematic views illustrating waveforms of outputs of first detector (110), a second detector (120), a switch controller (131) and a 2-bit switch (132) at first to sixth modes.

DETAILED DESCRIPTION

Various exemplary embodiments will be described more fully hereinafter with reference to the accompanying drawings, in which some exemplary embodiments are shown. The present inventive concept may, however, be embodied in many different forms and should not be construed as limited to the example embodiments set forth herein. Rather, the described aspect is intended to embrace all such alterations, modifications, and variations that fall within the scope and novel idea of the present disclosure.

Hereinafter, exemplary embodiments of the present disclosure will be described in detail with reference to the accompanying drawings.

The input signal simplification device according to an exemplary embodiment of the present disclosure is applied to a PLC high speed counter to enhance a processing speed by simplifying signals of 6 types of modes. Thus, operations of 6 types of modes in MPU (30) of FIG. 1 will be described in detail in the first place.

FIGS. 3a to 3f, as explained in the foregoing, are schematic views illustrating six different input modes and operations thereof according to types of encoders.

FIG. 3a illustrates a first mode of 1-phase/2-input/1-multiplication method, where a counter is added when a B-phase input pulse is OFF, and a rising edge is generated on A phase, and a counter is deducted when a B-phase input pulse is ON, and a falling edge is generated on A phase.

FIG. 3b illustrates a second mode of 1-phase/2-input/2-multiplication method, where a counter is added when a B-phase input pulse is OFF, and a rising edge is generated on A phase, a counter is added, and a counter is deducted when a falling edge is generated. Furthermore, a counter is deducted when a B-phase input pulse is ON and a rising edge is generated on A phase, and a counter is added when a falling edge is generated.

FIG. 3c illustrates a third mode of CW/CCW method, where a counter is added only when a B-phase input pulse is OFF, and a rising edge is generated on A phase, and a counter is deducted only when a A-phase input pulse is OFF, and a rising edge is generated on B phase.

FIG. 3d illustrates a fourth mode of 2-phase/1-multiplication method, where a counter is added when a rising edge is generated on A phase and phase of A phase is ahead by calculating a phase difference between phases of A phase and B phase, and a counter is deducted when a falling edge is generated and phase of B phase is ahead.

FIG. 3e illustrates a fifth mode of 2-phase/2-multiplication method, where a counter is added when a rising edge is generated on A phase and phase of A phase is ahead by calculating a phase difference between phases of A phase and B phase, and a counter is deducted when a falling edge is generated. Furthermore, a counter is deducted when a rising edge is generated on A phase and phase of B phase is ahead, and a counter is deducted when a falling edge is generated.

FIG. 3f illustrates a sixth mode of 2-phase/4-multiplication method, where a counter is added whenever a rising or falling edge is generated on A phase or B phase, and phase

through the AND gate may become an output of the first detector (110) by being combined as one single signal by OR gate.

The second detector (120) may output a pulse string having extracted the rising or falling edge for actually performing the addition or deduction calculation, using the first and second inputs and output of the first detector (110) as inputs. To be more specific, the second detector (120) can extract a case of actually performing the addition or deduction calculation in response to each operation mode of the PLC high speed counter among all rising or falling edges of reference signal which is a reference of addition or deduction inputted from the first detector (110). The second detector (120) can extract only the pulse that actually performs the addition or deduction through state signal information that shows a condition for actually realizing the addition or the deduction from the first input and the second input.

Now, a configuration of the switching unit (130) in the apparatus for simplification of input signal (the apparatus) according to an exemplary embodiment of the present disclosure will be described.

The switching unit (130) of the apparatus may include a switching controller (131) and a 2-bit switch (132).

The switching controller (131) can extract only the state signal in response to each mode from the first and second inputs. The switch controller (131) may be formed by D flip-flop, two AND elements and one OR element, but may be realized by other various elements in addition thereto.

The 2-bit switch (132) may output a pulse signal to a first output when addition calculation is performed using a signal of the switch controller (131) and an output of the second detector (120), and output a pulse signal to a second output when deduction calculation is performed. That is, the 2-bit switch (132) may output a pulse signal in response to the addition calculation or the deduction calculation outputted by the second detector (120) by dividing the pulse signal to an addition calculation pulse and a deduction pulse signal, using, as a control signal, a state signal showing the addition and deduction states at the switch controller (131). A universal output port of MPU (30) may be used for control of logic circuit of the apparatus for simplification of input signal according to an exemplary embodiment of the present disclosure.

FIG. 10 is a schematic view illustrating a universal output port value, per input mode, of MPU (30) for logic circuit control in an apparatus (100) for simplification of input signal according to an exemplary embodiment of the present disclosure.

The universal output port value of FIG. 10 operates to a designed circuit of FIG. 8 and may be changed by a circuit change to an appropriate logic value. That is, when inner circuits of the first detector, the second detector and switching unit which are basic elements of the present disclosure are changed, it is preferable that the universal output port value of FIG. 10 be appropriately changed.

FIGS. 11 to 16 are schematic views illustrating waveforms of outputs of first detector (110), a second detector (120), a switch controller (131) and a 2-bit switch (132) at first to sixth modes.

Referring to FIG. 11, in case of first mode, i.e., in case of 1-phase/2-input/1-multiplication mode, it can be noted that an output of the first detector (110) generates a single pulse at every rising or falling edge on A phase which is a reference signal of first mode. Furthermore, it can be noted that an output of the second detector (120) is detected only

in case of falling edge on A phase when a B phase signal is OFF and a rising edge of A phase or a B phase signal is ON.

It can be also noted that an output of the switch controller (131) equally outputs a B phase signal in response to B phase state which is a state signal of first mode.

Furthermore, it can be noted that an output of 2-bit switch (132), outputted by using, as input, an output of the second detector (120) and an output of the switch controller (131), is classified into a first output and a second output, and an output signal of the second detector (120) is outputted by being divided according to addition calculation and deduction calculation in response to the output of the switch controller (131).

Referring to FIG. 12, it can be noted that, in case of second mode, i.e., in case of 1-phase/2-input/2-multiplication mode, an output of the second detector (120) generates a single pulse at every rising or falling edge on A phase which is a reference signal of second mode. Furthermore, an output of the second detector (120) is a pulse string of rising or falling edge performing an actual addition or deduction calculation among the outputs of the first detector (110).

However, in case of 1-phase/2-input/2-multiplication mode, an output of the first detector (110) and an output of the second detector (120) are same, because one calculation is performed out of the addition and deduction calculations in response to B phase signal at every rising or falling edge on A phase.

It can be noted that an output of the switch controller (131) is same as the B phase signal which is state signal of second mode, and an output of the 2-bit switch (132) which is a final output is divided to a first output and a second output, and an output signal of the second detector (120) is outputted by being divided to addition or deduction calculation in response to the output of the switch controller (131).

Referring to FIG. 13, it can be noted that, in case of third mode, i.e., in case of CW/CCW mode, an output of the first detector (110) is an A phase signal and a B phase signal each of which is a reference signal of third mode, and addition or deduction calculation is performed only at the rising edges thereof such that a single signal is generated at every rising edge on A phase and every falling edge of B phase.

Furthermore, it can be also noted that an output of the second detector (120) is such that only a pulse of rising edge on A phase is detected when A phase and B phase signals which are state signals of third mode are OFF, and only a pulse of rising edge on B phase is detected when an A phase signal is OFF. An output of the switch controller (131) is outputted as a toggling signal whenever A phase signal and B phase signal which are state signals of third mode are changed.

It can be noted that an output of the 2-bit switch (132) which is a final output, is divided to a first output and a second output, and an output signal of the second detector (120) is outputted by being divided to addition and deduction calculation in response to output of the switch controller (131).

Referring to FIG. 14, it can be noted that in case of fourth mode, i.e., in case of 2-phase/1-multiplication mode, an output of the first detector (110) generates a pulse at every rising or falling edge of A phase signal which is a reference signal of fourth mode.

Furthermore, it can be noted that an output of the second detector (120) is such that remaining pulses are excluded except for when A phase is ahead of B phase in response to a phase difference between A phase and B phase which are

state signals, and a rising edge is generated on A phase, and when B phase is ahead of A phase and a falling edge is generated on A phase.

An output of the switch controller (131) is such that a control signal is outputted capable of discerning addition and deduction states when a low signal is outputted when A phase is ahead of B phase, and a high signal is outputted when B phase is ahead of A phase.

It can be noted that an output of the 2-bit switch (132) is divided to a first output and a second output, and an output signal of the second detector (120) is outputted by being divided to addition and deduction calculations in response to an output of the switch controller (131).

Referring to FIG. 15, it can be noted that, in case of fifth mode, i.e., in case of 2-phase/2-multification mode, an output of the first detector (110) generates a pulse at every rising and falling edge of A phase signal which is a reference signal of the fifth mode.

Furthermore, an output of the second detector (120) is such that remaining pulses are excluded except for when A phase is ahead of B phase in response to a phase difference between A phase and B phase which are state signals, and a rising edge is generated on A phase, and when B phase is ahead of A phase and a falling edge is generated on A phase.

An output of the switch controller (131) is such that a control signal is outputted capable of discerning addition and deduction states when a low signal is outputted when A phase is ahead of B phase, and a high signal is outputted when B phase is ahead of A phase.

It can be noted that an output of the 2-bit switch (132) is divided to a first output and a second output, and an output signal of the second detector (120) is outputted by being divided to addition and deduction calculations in response to an output of the switch controller (131).

Referring to FIG. 16, in case of sixth mode, i.e., in case of 2-phase/4-multification mode, an output of the first detector (110) generates a pulse at every rising and falling edge of A phase and B phase which are reference signals of the sixth mode. Furthermore, it can be noted that an output of the second detector (120) is remained only with a pulse of a moment where actual addition or deduction calculation is performed out of output of the first detector (110).

However, in case of sixth mode, an output of the first detector (110) and an output of the second detector (120) are same, because addition calculation or deduction calculation is performed at every rising or falling edge on A phase.

It can be noted that an output of the switch controller (131) outputs a low signal and a high signal respectively by dividing a case where a phase on A phase is ahead of a phase of B phase, and a case where a phase on B phase is ahead of a phase of A phase.

It can be noted that an output of the 2-bit switch (132) is divided to a first output and a second output, and an output of the second detector (120) is outputted by being divided to addition calculation and deduction calculation in response to the output of the switch controller (131).

As discussed in the foregoing, the apparatus for simplification of input signal according to an exemplary embodiment of the present disclosure can change an input signal of six modes to an addition signal formed with a single pulse and a deduction signal.

Although the present disclosure has been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and

embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure.

More particularly, various variations and modifications are possible in the component parts and/or arrangements of subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

What is claimed is:

1. An apparatus for simplification of input signal configured to input, to an MPU (Micro Processing Unit), an output of an input circuit at a PLC high speed counter module by converting the input to a single signal, the apparatus comprising:
  a first detector configured to output a single pulse in response to a rising edge or a falling edge by detecting the rising edge or the falling edge of a reference signal, which is a reference of adding or deducting calculation in response to an operation mode of the high speed counter module;
  a second detector configured to detect, from an output of the first detector, a pulse of rising edge or falling edge configured to perform an actual adding or deducting calculation in response to an operation mode of the high speed counter module; and
  a switching unit configured to output an output of the second detector using the adding or deducting calculation.

2. The apparatus of claim 1, wherein a control signal is transmitted to the first, second detectors and the switching unit by using a general output port of the MPU.

3. The apparatus of claim 1, wherein the operation mode includes any one mode of a first mode of 1-phase/2-input/ 1-multiplication method, a second mode of 1-phase/2-input/ 2-multiplication method, a third mode of CW/CCW method, a fourth mode of 2-phase/1-multiplication method, a fifth mode of 2-phase/2-multiplication method and a sixth mode of 2-phase/4-multiplication method.

4. The apparatus of claim 1, wherein the switching unit includes a 2-bit switch configured to perform a one-on-one connection or a cross connection in response to a control signal by receiving a 2-bit input, and a switch controller configured to control the 2-bit switch by outputting through adding or deducting calculation in response to the operation mode.

5. The apparatus of claim 1, wherein the first detector includes a first oscillation unit configured to output a signal pulse by detecting a rising edge of a first input, a second oscillation unit configured to output a signal pulse by detecting a falling edge of a first input, a third oscillation unit configured to output a signal pulse by detecting a rising edge of a second input, a fourth oscillation unit configured to output a signal pulse by detecting a falling edge of a second input, and an edge detector configured to detect only an output of a reference signal from the first to fourth oscillation units in response to the operation mode.

6. The apparatus of claim 5, wherein the edge detector removes an input which is not a reference signal in response to the operation mode.

7. The apparatus of claim 5, wherein the edge detector combines outputs corresponding to the reference signal in response to the operation mode.

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